PREPARED BY : DATE	SHARP	SPEC No. LD-12511B
		FILE No.
APPROVED BY : DATE		ISSUE: July.13. 2000
		PAGE: 27 pages
	TFT LIQUID CRYSTAL DISPLAY GROUP SHARP CORPORATION	APPLICABLE GROUP TFT LIQUID CRYSTAL DISPLAY GROUP
	SPECIFICATION	

DEVICE SPECIFICATION FOR

TFT-LCD Module

MODEL No.

LQ141F1LH02

☐ CUSTOMER'S APPROVAL

DATE

BY

PRESENTED

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RECORDS OF REVISION

LQ141F1LH02

SPEC No.	DATE	REVISED No.	PAGE	SUMMARY	NOTE
LD-12511	Jul. 13. 2000	-	-		1st Issue
LD-12511A	Nov. 16. 2000	A	2	"INV is built in this module" added	2nd Issue
			5	4-3 CN1 → CN3 changed.	
				CONNECTOR parts no. changed.	
				Pin no. and ID no. changed.	
				5 VBB, VBC, SDA, SCL, FPVEE spec. changed	
			6	6-1 Current dissipation changed	
			7	6-2.1 [Note] I1 and ② deleted, SDA added	
				6.2.2 VBB spec Added.	
				VBC typ spec. added	
			8	6.2.3 IVIN condition separated	
				FPVEE spec Changed	
				6.2.4 sequence Changed	
				6.2.5 fig Changed	
				6.2.6 The condition of shut down changed	
			9	6.2.7 Brightness spell changed	
			12	7-1, 7-2 chenged to ENAB ONLY MODE	
			15	9. 25th byte changed	
			18	10 Luminance of white SMB → SDA changed	
				typical condition changed	
			21	15-1 In Barcode label(module), sharp	
				specification is changed	
			22	15-1 Printing specification of sharp	
				Specification is added.	
			23	15-2 Printing specification of DELL	
				packing label is added.	
			25	Location of barcode label attachment is	
				added.	
			26	CONNECTOR 3 parts no. changed	
				Inverter size changed	
LD-12511B	Mar. 22. 2001	B	26	Mounting hole spec is updated(2.3->2.5mm)	3rd Issue

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Do not use the device for equipment that requires an extreme level of reliability, such as aerospace applications, telecommunication equipment(trunk lines), nuclear power control equipment and medical or other equipment for life support.

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Contact and consult with a SHARP sales representative for any questions about this device.

1. Application

This specification applies to a color TFT-LCD module, LQ141F1LH02.

2. Overview

This module is a color active matrix LCD module incorporating amorphous silicon TFT (Thin Film Transistor). This module is based on the standards of SPWG(Standard Panels Working Group).

It is composed of a color TFT-LCD panel, driver ICs, control circuit and power supply circuit and a backlight unit. Graphics and texts can be displayed on a 1400×3×1050 dots panel with 262,144 colors by using LVDS (Low Voltage Differential Signaling) to interface and supplying +3.3V DC supply voltage for TFT-LCD panel driving and supply voltage for backlight.

The TFT-LCD panel used for this module has very high aperture ratio. A low-reflection and higher-color-saturation type color filter is also used for this panel. Therefore, high-brightness and high-contrast image, which is suitable for the multimedia use, can be obtained by using this module.

Optimum viewing direction is 6 o'clock.

Backlight-driving DC/AC inverter is built in this module.

[Features]

1) High aperture panel ; high-brightness or low power consumption.
2) Brilliant and high contrast image.
3) Small footprint and thin shape.
4) Light weight.

3. Mechanical Specifications

Parameter	Specifications	Unit
Display size	36 (14.1") Diagonal	cm
Active area	285.6 (H)×214.2 (V)	mm
Pixel format	1400 (H)×1050 (V)	pixel
	(1 pixel = R+G+B dots)	
Pixel pitch	0.204(H)×0.204 (V)	mm
Pixel configuration	R,G,B vertical stripe	
Display mode	Normally white	
Unit outline dimensions *1	299.0(W)×228.0(H)×6.4max.(D)	mm
Mass *2	555±10	g
Surface treatment	Anti-glare and hard-coating 2H (Haze value = 25)	

*1.Note : excluding inverter unit and backlight cables.

*2.Note : including inverter unit

Outline dimensions is shown in Fig.1

4. Input Terminals

4-1. TFT-LCD panel driving

CN1 (LVDS signals and +3.3V DC power supply)

Using connector : FI-XB30S-HF10 (JAE)

Corresponding connector : FI-X30M, or FI-X30H (JAE)

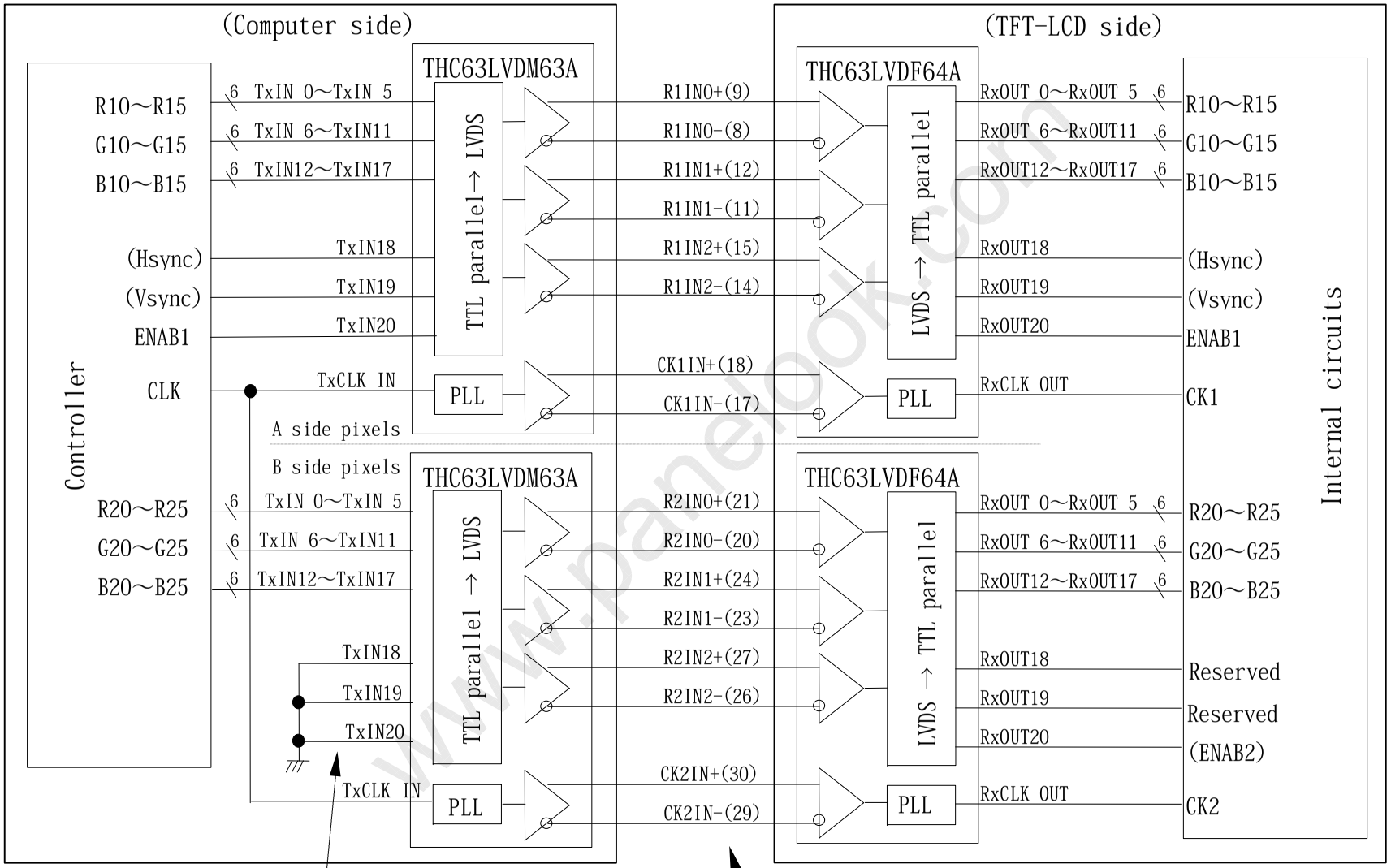
Pin No.	Symbol	Function	Remark
1	GND		
2	Vcc	+3.3V power supply	
3	Vcc	+3.3V power supply	
4	Vedid	DCC +3.3V power supply	
5	NC	Reserved	
6	CLKedid	DDC Clock	
7	DATAedid	DDC Data	
8	R1IN0-	Receiver signal of A side pixels (-)	LVDS
9	R1IN0+	Receiver signal of A side pixels (+)	LVDS
10	GND		
11	R1IN1-	Receiver signal of A side pixels (-)	LVDS
12	R1IN1+	Receiver signal of A side pixels (+)	LVDS
13	GND		
14	R1IN2-	Receiver signal of A side pixels (-)	LVDS
15	R1IN2+	Receiver signal of A side pixels (+)	LVDS
16	GND		
17	CK1IN-	Clock signal of A side pixels (-)	LVDS
18	CK1IN+	Clock signal of A side pixels (+)	LVDS
19	GND		
20	R2IN0-	Receiver signal of B side pixels (-)	LVDS
21	R2IN0+	Receiver signal of B side pixels (+)	LVDS
22	GND		
23	R2IN1-	Receiver signal of B side pixels (-)	LVDS
24	R2IN1+	Receiver signal of B side pixels (+)	LVDS
25	GND		
26	R2IN2-	Receiver signal of B side pixels (-)	LVDS
27	R2IN2+	Receiver signal of B side pixels (+)	LVDS
28	GND		
29	CK2IN-	Clock signal of B side pixels (-)	LVDS
30	CK2IN+	Clock signal of B side pixels (+)	LVDS

【Note 1】Relation between LVDS signals and actual data shows below section (4-2).

【Note 2】The shielding case is connected with signal GND

4-2 Interface block diagram

Using receiver：THC63LVDF64A (THINE)、Corresponding Transmitter：THC63LVDM63A (THINE）, DS90C363,DS90C383(National semiconductor)



4-3. Inverter connector pin assign

CN3 : (Inverter signals and Inverter Power Supply)

Using connector : WR-L16SB-VF-HD2-1 (JAE)

Corresponding connector: WR-KL16P-VF (JAE)

Pin no.	Symbol	Function
1,2,4	V_{IN}	Inverter power supply voltage
3,5,6	GND	Gnd
7	VBB	Base of Brightness control voltage
8	VBC	Brightness control IC supply voltage
9	SDA	Brightness control serial data signal
10	SCL	Brightness control serial clock signal
11	FPVEE	Backlighgt on/off signal
12	N.C.	This is electrically opened
13	PANEL_ID3	Panel identity bit3 =1
14	PANEL_ID2	Panel identity bit2 =0
15	PANEL_ID1	Panel identity bit1 =0
16	PANEL_ID0	Panel identity bit0 =0

5. Absolute Maximum Ratings

Parameter	Symbol	Condition	Ratings	Unit	Remark
Input voltage	V_I	Ta=25℃	−0.3 ～ Vcc+0.3	V	【Note1】
+3.3V supply voltage	Vcc	Ta=25℃	0 ～ ＋ 4	V	
Storage temperature	Tstg	—	−25 ～ ＋60	℃	【Note2】
Operating temperature	Topa	—	0 ～ ＋50	℃	
Inverter supply voltage	V_{IN}	Ta=25℃	−0.5～ ＋ 25	V	
Brightness control IC supply voltage	VBC	Ta=25℃	−1.0～ ＋ 7.0	V	
Inverter signals	VBB, SDA,SCL	Ta=25℃	−1.0～ ＋ 7.0	V	
	FPVEE	Ta=25℃	−0.5～ ＋ 7.0	V	

【Note1】LVDS signals

【Note2】Humidity：95%RH Max. at Ta≦40℃.

Maximum wet-bulb temperature at 39℃ or less at Ta>40℃.

No condensation.

6. Electrical Characteristics

6-1.TFT-LCD panel driving Ta＝25℃

Parameter			Symbol	Min.	Typ.	Max.	Unit	Remark
Vcc	Supply voltage		Vcc	+3.0	+3.3	+3.6	V	【Note2】
	Current dissipation		Icc	—	720	1240	m A	【Note3】
Permissive input ripple voltage			V_{RP}	—	—	100	mV p-p	Vcc=+3.3V
Input voltage range			V_I	0	—	2.4	V	LVDS signal
Differential input threshold voltage		High	V_{TH}	—	—	+100	mV	V_{CM}=+1.2V 【Note1】
		Low	V_{TL}	–100	—	—	mV	
Input current (High)			I_{OH}	—	—	±10	μA	V_I=2.4V Vcc=3.6V
Input current (Low)			I_{OL}	—	—	±10	μA	V_I=0V Vcc=3.6V
Terminal resistor			R_T	—	100	—	Ω	Differential input

【Note1】 V_{CM} : Common mode voltage of LVDS driver.

【Note2】

On-off conditions for supply voltage

Vcc rise time

t1≦10 ms

Vcc on time before signal on

0≦t2≦50 ms

Vcc on time after signal off

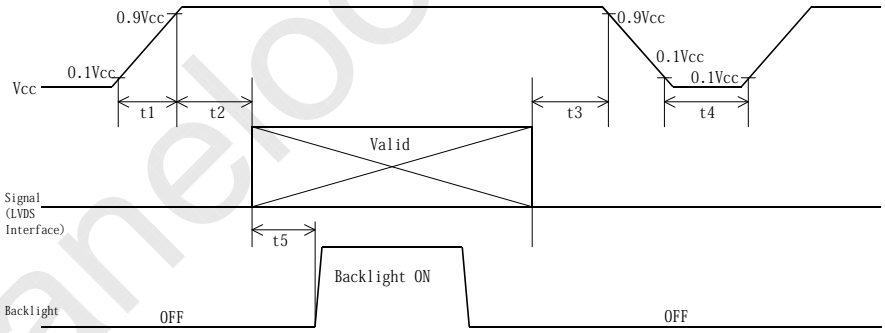
0≦t3≦50 ms

Shut down period of Vcc

400ms≦t4

Signal on time before Backlight on

200ms≦t5



Power sequence for Backlight is especially not specified , however it is recommended to consider some timing difference between LVDS input and Backlight input as shown above.

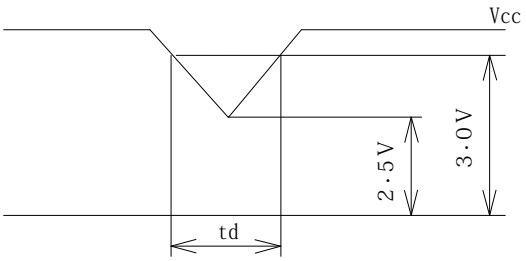
If the Backlight lights on before LCD starting, or if the Backlight is kept on after LCD stopping, the screen may look white for a moment or abnormal image may be displayed.

This is caused by variation in output signal from timing generator at LVDS input on or off. It does not cause the damage to the LCD module.

Vcc-dip conditions

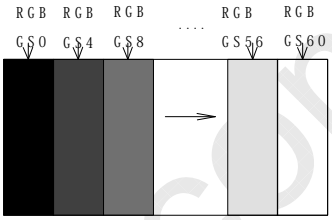
1) 2.5 V≦Vcc＜3.0 V
td≦10 ms

2) Vcc＜2.5 V



Vcc-dip conditions should also follow the On-off conditions for supply voltage

【Note3】 Typical current situation : 16-gray-bar pattern.
Vcc=+3.3V



6-2. Inverter driving

6-2.1.Backlight life time

The backlight system is an edge-lighting type with single CCFT (Cold Cathode Fluorescent Tube). The life time of the lamp are shown in the following table.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Lamp life time	L_L	10000	—	—	Hour	【Note】

【Note】 Lamp life time is defined as the time when ① occurs in the continuous operation under the condition of Ta = 25℃ and SDA data=00_{HEX}

① Brightness becomes 50 % of the original value under standard condition.

6.2.2. Recommended Operating Condition

Parameter	Symbol	Min.	Typ	Max	Unit
Inverter power supply voltage	V_{IN}	9	—	21	V
Base of Brightness control voltage	VBB	4.85	5.0	5.2	V
Brightness control IC supply voltage	VBC	4.5	5.0	5.5	V
Logic signals	SDA,SCL FPVEE	0		5	V

6.2.3. DC Electrical Conditions Ta=25℃

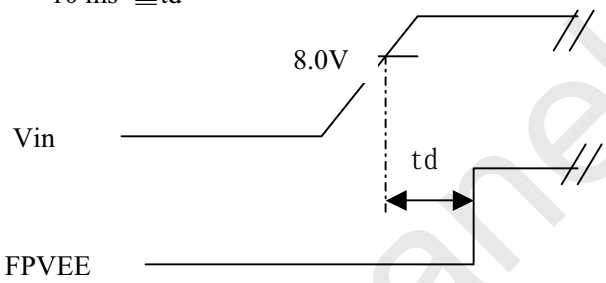
Parameter		Symbol	Condition	Min.	Typ	Max	Unit	Remark
V_{IN} supply current		IV_{IN}	V_{IN}= 9 V,VBB=5V	290	—	585	mA	Note
			V_{IN}=21V,VBB=5V	120	—	310		
Brightness control IC supply current		I_{VBC}	VBC =4.5～5.5V	—	—	200	uA	
SDA SCL	Input voltage low	V_{IL}	VBC =4.5～5.5V	—	—	0.3× VBC	V	
	Input voltage High	V_{IH}	VBC =4.5～5.5V	0.7× VBC	—	—	V	
FPVEE	Input voltage low	V_{IL}	V_{IN}=12V	0	—	0.6	V	
	Input voltage High	V_{IH}	V_{IN}=12V	3.0	—	5.0	V	

Note：Brightness control from minmum to maxmaum

6.2.4. Power ON/OFF sequence

9 V≦Vin＜21 V

10 ms ≦td



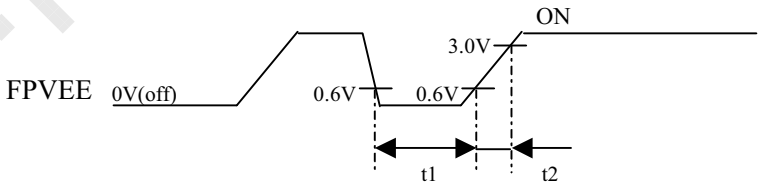
6.2.5. FPVEE ON sequence

Backlight power on/off is possible with FPVEE.

Make sure to have more than 50 millisecond interval between each power-on.

50 m s ≦ t1

t2 ≦ 20 ms



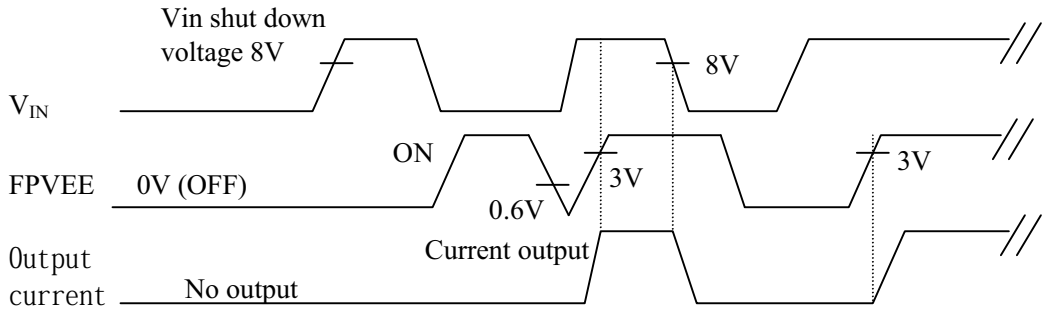
6.2.6. The Condition of Shut Down

Please refer to the figure below for the conditions that will cause the inverter shut down.

If the V_{IN} voltage is higher than 8.0V but there is no enable signal, then the inverter will shut down.

If the V_{IN} voltage is down less than 8.0V ,it will cause the inverter shut down.

The enable signal has to be reset to get the inverter started again.



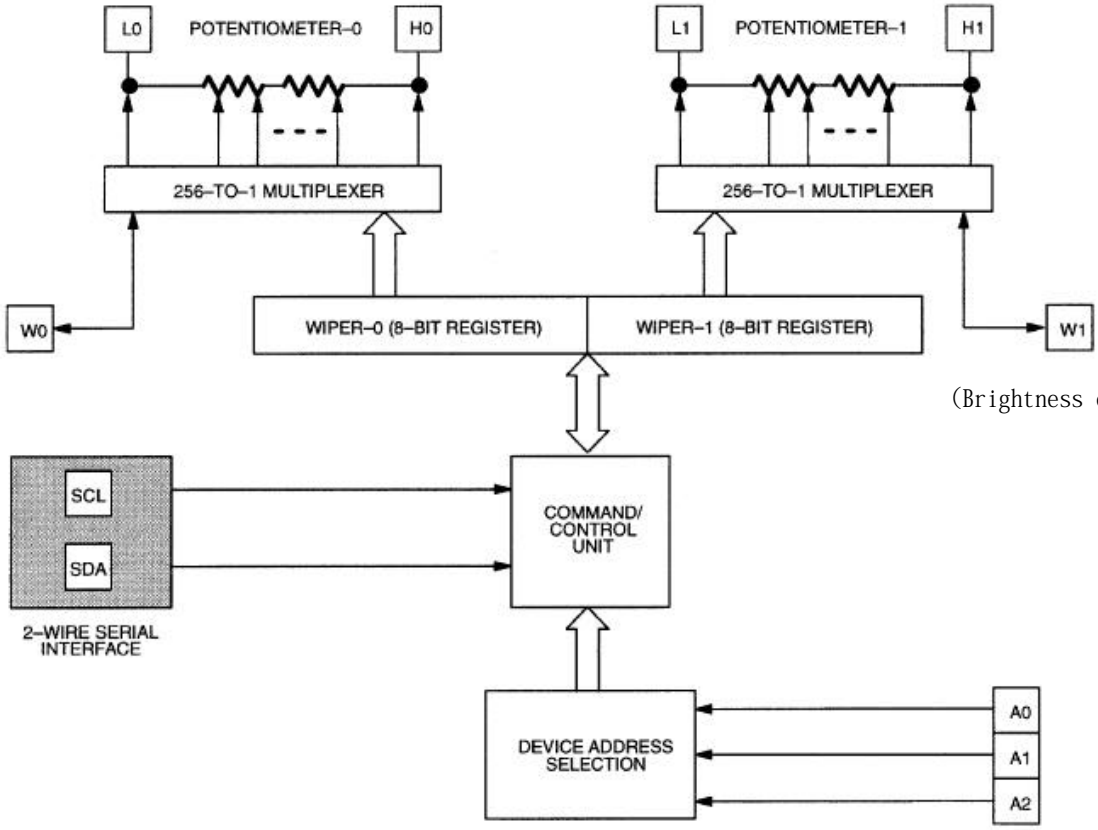
6.2.7. Brightness Control

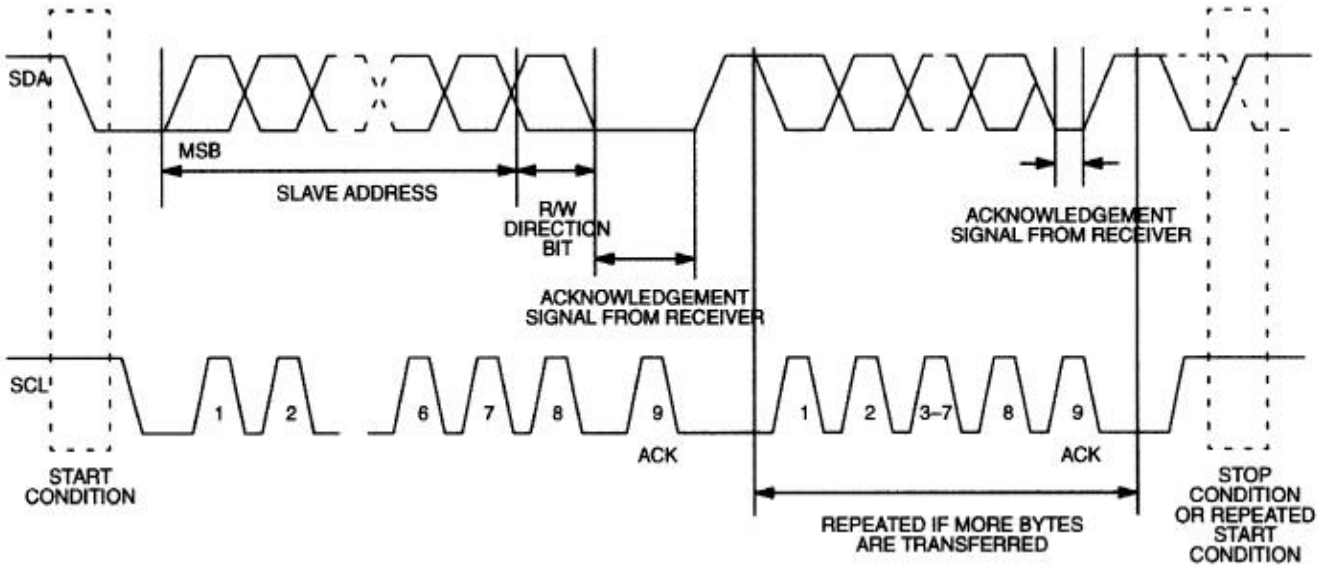
SDA data	Brightness	Notes
00_{HEX}	Maxmum Brightness	Set on power-up
0 1 ～FE_{HEX}	↓	
FF_{HEX}	Minimum Brightness	

Block diagram

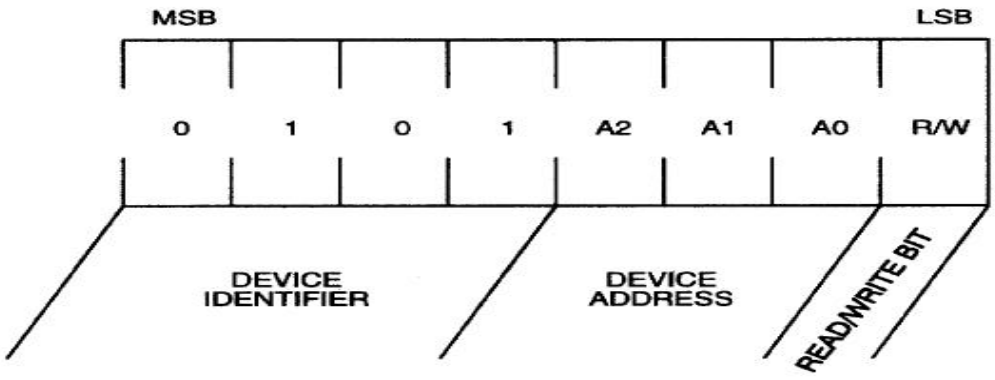
Note：(A2,A1,A0)=(0,0,0)

WIPER0 is not using

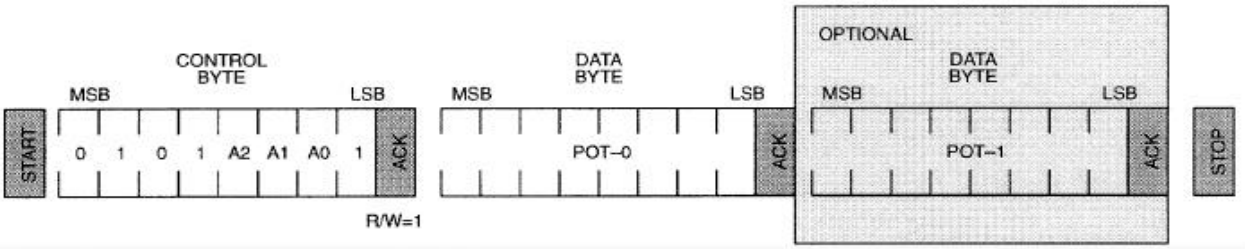




Brightness control byte

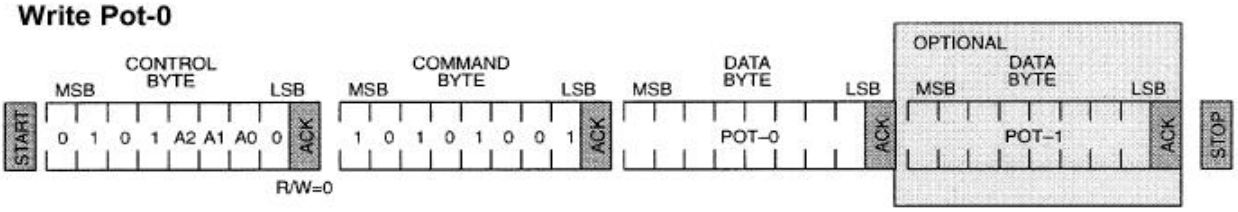


Brightness control data read protocols

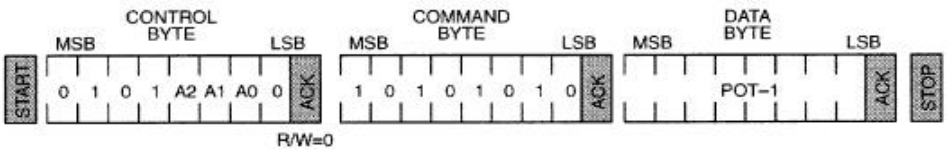


Brightness control data wright protocols

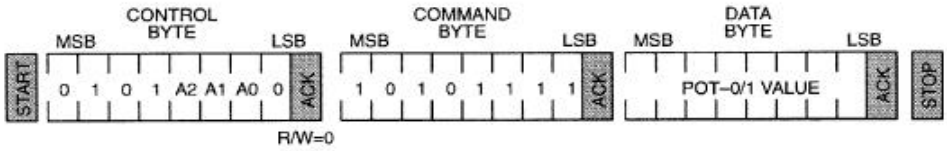
Write Pot-0



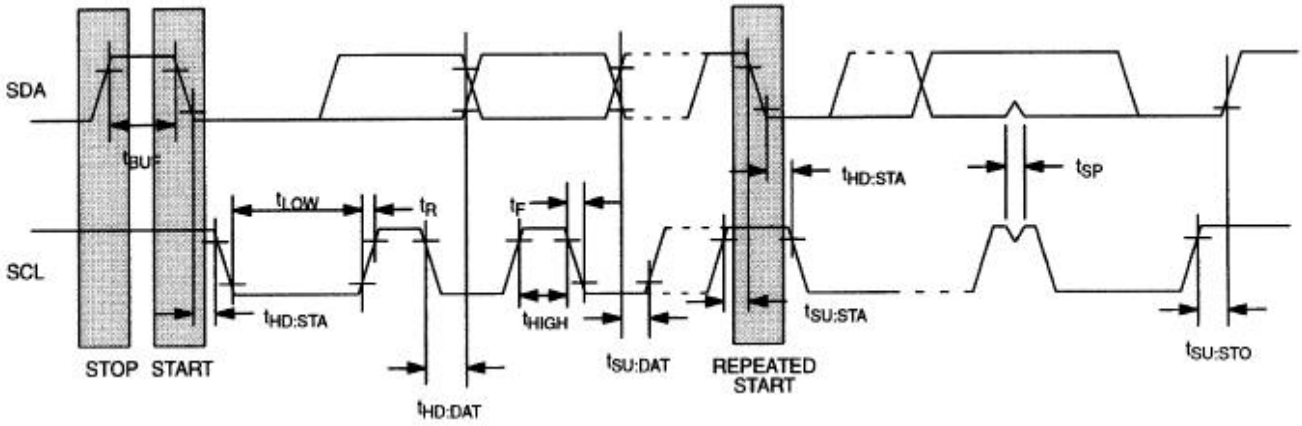
Write Pot–1



Write Pot–0/1 (same value)



Timing daigram



6.2.8. AC Electrical Characteristic 0℃～50℃ VBC＝5.0V

PARAMETER		SYMBOL	MIN.	MAX	UNIT	NOTE
Pulse width of spikes		t_{sp}		50	ns	
SCL clock frequency	fast mode	f_{SCI}	0	400	kHz	1
	Standard mode		0	100		2
BUS free time between STOP and START condition	fast mode	t_{BUF}	1.3		us	
	Standard mode		4.7			
Hold time (Repeated) START condition	fast mode	$t_{HD;STA}$	0.6		us	3
	Standard mode		4.0			
Low Period of SCL CLOCK	fast mode	t_{LOW}	1.3		us	
	Standard mode		4.7			
High Period of SCL CLOCK	fast mode	t_{HIGH}	0.6		us	
	Standard mode		4.0			
Data hold time	fast mode	$t_{HD;DAT}$	0	0.9	us	
	Standard mode		0			
Data setup time	fast mode	$t_{SU;DAT}$	100		ns	
	Standard mode		250			
Rise time of both SDA and SCL signals	fast mode	t_R		300	ns	
	Standard mode			1000		
Fall time of both SDA and SCL signals	fast mode	tr		300	ns	
	Standard mode			300		
Setup time for STOP condition	fast mode	$t_{SU;STO}$	0.6		us	
	Standard mode		4.0			

NOTES:

1.fast mode.(400kHz clock rate)

2.Standard mode.(100kHz clock rate)

3.After this period, the first clock pulse is generated.

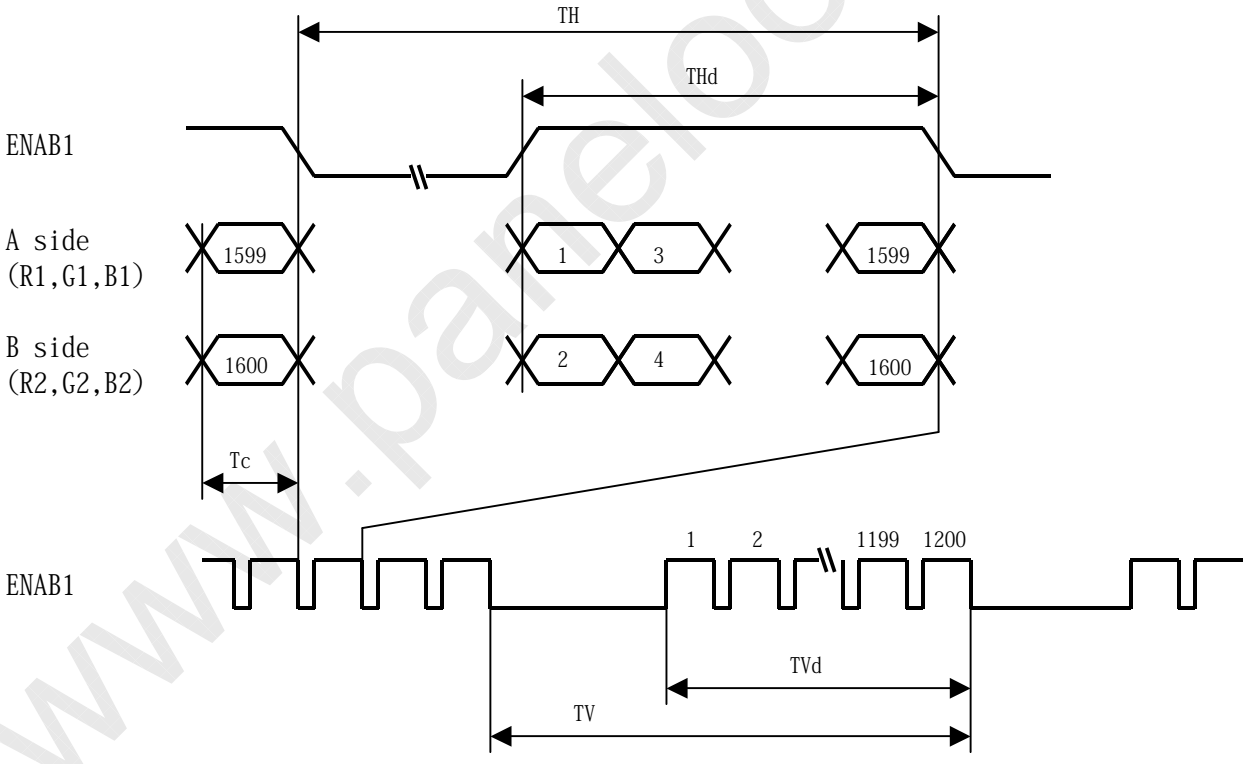
7. Timing characteristics of input signals

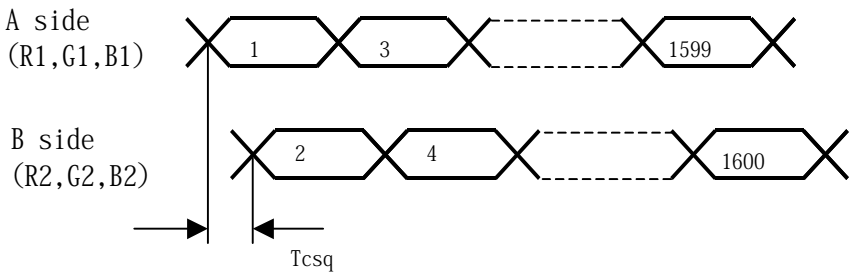
7-1. Timing characteristics

Parameter		Symbol	Min.	Typ.	Max.	Unit	Remark
Clock	Frequency	1/Tc	40	54	56	MHz	
	Skew	Tcsq	-2	0	-2	ns	【Note1】
Data enable Signal	Horizontal period	TH	800	844	1044	clock	
			14.8	15.6	—	μs	
	Horizontal period (High)	THd	700	700	700	clock	
	Vertical period	TV	1054	1066	1080	line	【Note2】
			15.61	16.67	—	ms	
	Vertical period (High)	TVd	1050	1050	1050	line	

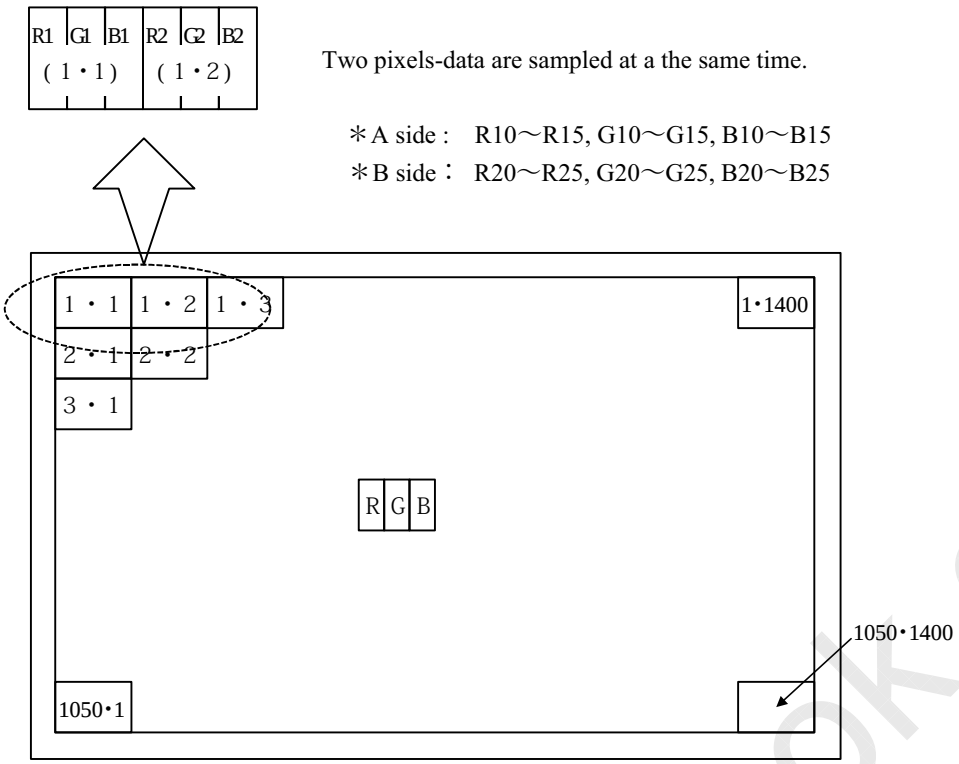
【Note1】 Lvds (A Side data)– Lvds (B side data) phase difference

【Note2】 In case of using the long vertical period, the deterioration of display quality, flicker, etc., may occur.





7-3. Input Data Signals and Display Position on the screen



Two pixels-data are sampled at a the same time.

＊A side : R10～R15, G10～G15, B10～B15

＊B side： R20～R25, G20～G25, B20～B25

Display position of input data (V・H)

8. Input Signals, Basic Display Colors and Gray Scale of Each Color

	Colors & Gray scale	Data signal																		
		GrayScale	R10	R11	R12	R13	R14	R15	G10	G11	G12	G13	G14	G15	B10	B11	B12	B13	B14	B15
			R20	R21	R22	R23	R24	R25	G20	G21	G22	G23	G24	G25	B20	B21	B22	B23	B24	B25
Basic Color	Black	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	—	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Green	—	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Cyan	—	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Red	—	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Magenta	—	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	—	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	—	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale of Red	Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇧	GS1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Darker	GS2	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇧	↓				↓						↓						↓		
	⇩	↓				↓						↓						↓		
	Brighter	GS61	1	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	⇩	GS62	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red	GS63	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale of Green	Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇧	GS1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
	Darker	GS2	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
	⇧	↓				↓						↓						↓		
	⇩	↓				↓						↓						↓		
	Brighter	GS61	0	0	0	0	0	0	1	0	1	1	1	1	0	0	0	0	0	0
	⇩	GS62	0	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0
	Green	GS63	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Gray Scale of Blue	Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇧	GS1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
	Darker	GS2	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
	⇧	↓				↓						↓						↓		
	⇩	↓				↓						↓						↓		
	Brighter	GS61	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1
	⇩	GS62	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1
	Blue	GS63	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

0 : Low level voltage, 1 : High level voltage

Each basic color can be displayed in 64 gray scales from 6 bit data signals. According to the combination of total 18 bit data signals, the 262,144-color display can be achieved on the screen.

9. EDID data structure

This is the EDID(Extended Display Identification Data) data formats to support displays as defined in the VESA Plug & Display .

Byte (decimal)	Byte (hex)	Field Name and Comments	Value (hex)	Value (binary)
0	00	Header	00	00000000
1	01	Header	FF	11111111
2	02	Header	FF	11111111
3	03	Header	FF	11111111
4	04	Header	FF	11111111
5	05	Header	FF	11111111
6	06	Header	FF	11111111
7	07	Header	00	00000000
8	08	EISA manufacture code = SHP	4D	01001101
9	09	EISA manufacture code (Compressed ASCII)	10	00010000
10	0A	Product code (LQ141F1LH02 : ”5000”)	88	10001000
11	0B	Product code (hex,LSB first)	13	00010011
12	0C	LCD module Serial No (fixed “0”)	00	00000000
13	0D	LCD module Serial No (fixed “0”)	00	00000000
14	0E	LCD module Serial No (fixed “0”)	00	00000000
15	0F	LCD module Serial No (fixed “0”)	00	00000000
16	10	Week of manufacture (fixed “0”)	00	00000000
17	11	Year of manufacture - 1990 (ex 2000 – 1990 = 10) (fixed “0”)	00	00000000
18	12	EDID structure version # = 1	01	00000001
19	13	EDID revision # = 3	03	00000011
20	14	Video i/p definition = Digital i/p	80	10000000
21	15	Max H image size(cm) = 28cm	1C	00011100
22	16	Max V image size(cm) = 21cm	15	00010101
23	17	Display gamma (2.2×100) – 100 = 120	78	01111000
24	18	Feature support(stanby,suspend,RGB color/Prefer Time)	CA	11001010
25	19	Red/Green Low bit(RxRy/GxGy)	4E	01001110
26	1A	Blue/White Low bit(BxBy/WxWy)	80	10000000
27	1B	Red X(Rx) (written value “0.583”)	95	10010101
28	1C	Red Y(Ry) (written value “0.325”)	53	01010011
29	1D	Green X(Gx) (written value “0.308”)	4E	01001110
30	1E	Green Y(Gy) (written value “0.548”)	8C	10001100
31	1F	Blue X(Bx) (written value “0.150”)	26	00100110
32	20	Blue Y(By) (written value “0.117”)	1E	00011110
33	21	White X(Wx) (written value “0.313”)	50	01010000
34	22	White Y(Wy) (written value “0.329”)	54	01010100
35	23	Established timings 1 (800×600@60Hz)	00	00000000
36	24	Established timings 2 (1024×768@60Hz)	00	00000000
37	25	Established timings 3(Manufacture’s reserved timing)	00	00000000
38	26	Standard timing ID1 (Horizontal active pixels)	90	10010000
39	27	Standard timing ID1 (Aspect ratio 4:3)	40	01000000

40	28	Standard timing ID2	01	00000001
41	29	Standard timing ID2	01	00000001
42	2A	Standard timing ID3	01	00000001
43	2B	Standard timing ID3	01	00000001
44	2C	Standard timing ID4	01	00000001
45	2D	Standard timing ID4	01	00000001
46	2E	Standard timing ID5	01	00000001
47	2F	Standard timing ID5	01	00000001
48	30	Standard timing ID6	01	00000001
49	31	Standard timing ID6	01	00000001
50	32	Standard timing ID7	01	00000001
51	33	Standard timing ID7	01	00000001
52	34	Standard timing ID8	01	00000001
53	35	Standard timing ID8	01	00000001
54	36	Detailed timing descriptor#1 fck/10000 = 10800=2A30h	30	00110000
55	37	#1 fck	2A	00101010
56	38	#1 Horizontal active 1400 = 578h “78”	78	01111000
57	39	#1 Horizontal blanking 288 = 120h “20”	20	00100000
58	3A	#1 Horizontal active/Horizontal blanking “51h”	51	01010001
59	3B	#1 Vertical active 1050 = 41Ah “1A”	1A	00011010
60	3C	#1 Vertical blanking 16 = 010h “10”	10	00010000
61	3D	#1 Vertical active/Vertical blanking “40h”	40	01000000
62	3E	#1 Horizontal sync , offset 44 = 02Ch “2C”	2C	00101100
63	3F	#1 Horizontal sync , width 112 = 070h “70”	70	01110000
64	40	#1 Vertical sync,offset / Vertical sync,width	03	00000011
65	41	#1 Horizontal sync offset/width/Vertical sync offset/width	00	00000000
66	42	#1 Horizontal image size 285mm = 11Dh “1D”	1D	00011101
67	43	#1 Vertical image size 214mm = 0D6h “D6”	D6	11010110
68	44	#1 Horizontal image size / Vertical image size	10	00010000
69	45	Horizontal boader	00	00000000
70	46	Vertical boader	00	00000000
71	47	Flags	18	00011000
72	48	Detailed timing descriptor #2	00	00000000
73	49	Flag	00	00000000
74	4A	Reserved	00	00000000
75	4B	Dummy Descriptor	10	00010000
76	4C	Flag	00	00000000
77	4D	1st dummy	00	00000000
78	4E	2nd dummy	00	00000000
79	4F	3rd dummy	00	00000000
80	50	4th dummy	00	00000000
81	51	5th dummy	00	00000000
82	52	6th dummy	00	00000000
83	53	7th dummy	00	00000000

84	54	8th dummy	00	00000000
85	55	9th dummy	00	00000000
86	56	10th dummy	00	00000000
87	57	11th dummy	00	00000000
88	58	New line character #2 indicates end	0A	00001010
89	59	Padding with “blank” character	20	00100000
90	5A	Detailed timing descriptor #3	00	00000000
91	5B	Flag	00	00000000
92	5C	Reserved	00	00000000
93	5D	Dummy Descriptor	10	00010000
94	5E	Flag	00	00000000
95	5F	1st Dummy	00	00000000
96	60	2nd Dummy	00	00000000
97	61	3rd Dummy	00	00000000
98	62	4th Dummy	00	00000000
99	63	5th Dummy	00	00000000
100	64	6th Dummy	00	00000000
101	65	7th Dummy	00	00000000
102	66	8th Dummy	00	00000000
103	67	9th Dummy	00	00000000
104	68	10th Dummy	00	00000000
105	69	11th Dummy	00	00000000
106	6A	New line character #3 indicates end	0A	00001010
107	6B	Padding with “blank” character	20	00100000
108	6C	Detailed timing descriptor #4	00	00000000
109	6D	Flag	00	00000000
110	6E	Reserved	00	00000000
111	6F	Dummy descriptor	10	00010000
112	70	Flag	00	00000000
113	71	1st Dummy	00	00000000
114	72	2nd Dummy	00	00000000
115	73	3rd Dummy	00	00000000
116	74	4th Dummy	00	00000000
117	75	5th Dummy	00	00000000
118	76	6th Dummy	00	00000000
119	77	7th Dummy	00	00000000
120	78	8th Dummy	00	00000000
121	79	9th Dummy	00	00000000
122	7A	10th Dummy	00	00000000
123	7B	11th Dummy	00	00000000
124	7C	New line character #4 indicates end	0A	00001010
125	7D	Padding with “blank” character	20	00100000
126	7E	Extension flag	00	00000000
127	7F	Checksum	AC	10101100

10. Optical Characteristics

Ta=25℃, Vcc=+3.3V

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing angle range	Horizontal	θ21, θ22	CR>10	45	—	—	Deg.	【Note1,4】
	Vertical	θ11		10	—	—	Deg.	
		θ12		30	—	—	Deg.	
Contrast ratio		CRn	θ=0°	150	—	—		【Note2,4】
		CRo	Optimum viewing angle	—	300	—		
Response time	Rise	τr	θ=0°	—	15		ms	【Note3,4】
	Decay	τd		—	30		ms	
Chromaticity of white		x		—	0.313	—		【Note4】
		y		—	0.329	—		
Luminance of white 【Note4】		Y_{L1}		120	150	—	cd/m^2	Vin=21V SDA=00_{HEX}
White Uniformity		δ_W		—	—	1.45		【Note5】

※ The measurement shall be executed 30 minutes after lighting at rating. (typical condition: SDA=00_{HEX})

The optical characteristics shall be measured in a dark room or equivalent state with the method shown in Fig.2 below.

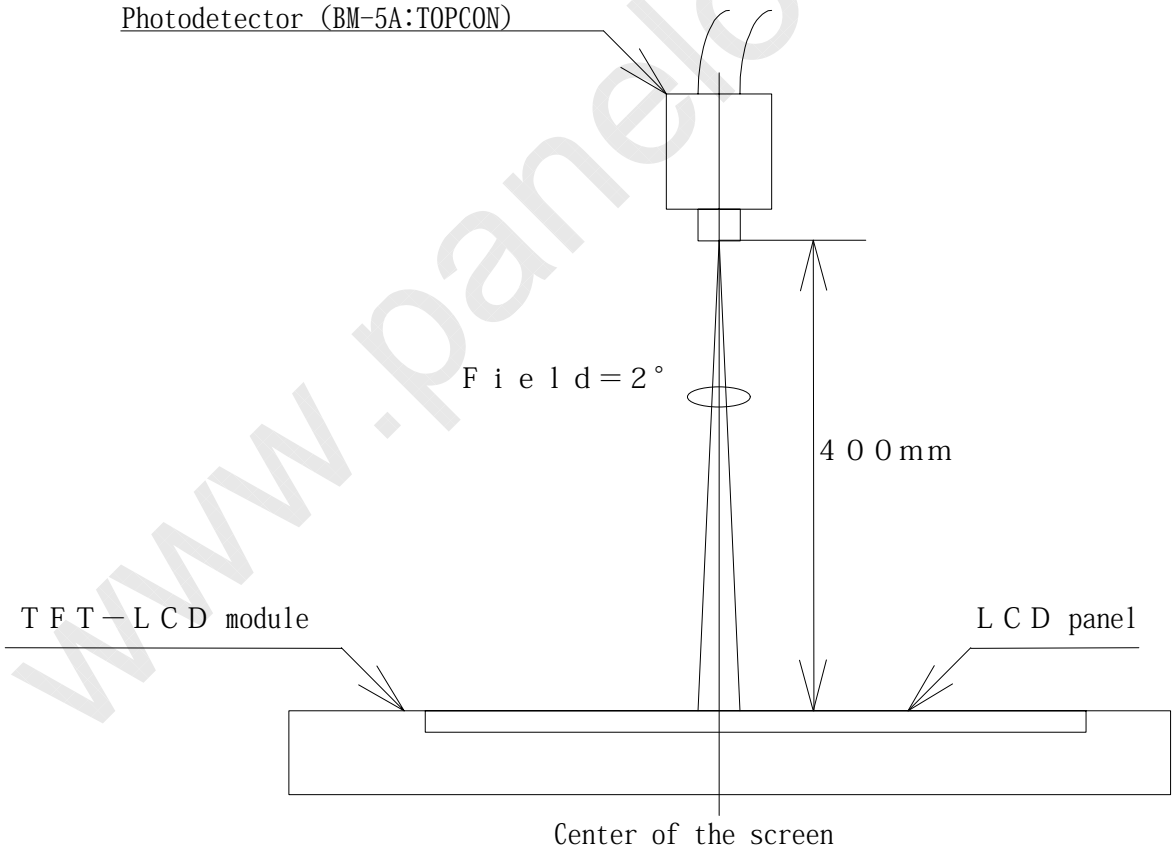
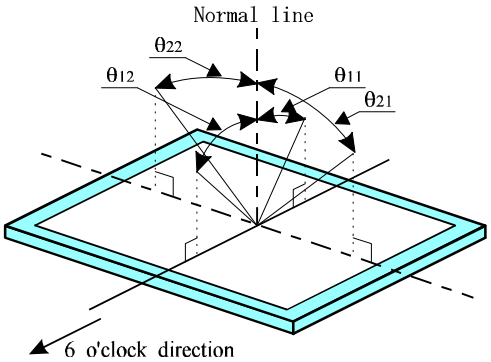


Fig.2 Optical characteristics measurement method

【Note1】Definitions of viewing angle range:



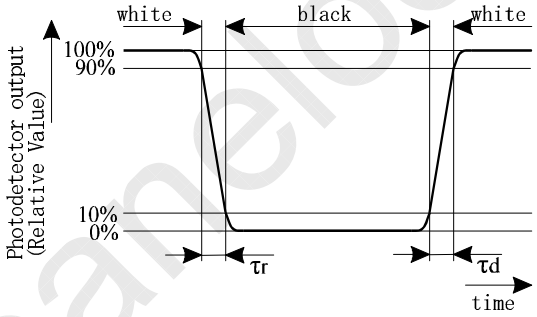
【Note2】Definition of contrast ratio:

The contrast ratio is defined as the following.

$$\text{Contrast Ratio (CR)} = \frac{\text{Luminance (brightness) with all pixels white}}{\text{Luminance (brightness) with all pixels black}}$$

【Note3】Definition of response time:

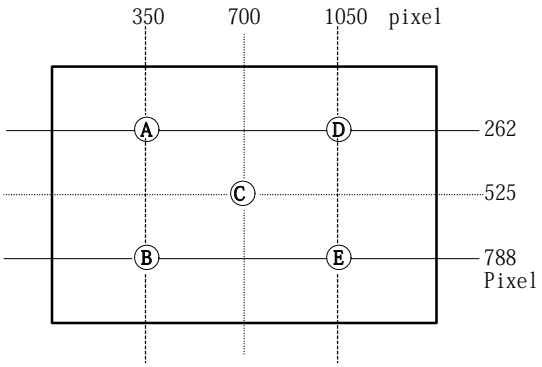
The response time is defined as the following figure and shall be measured by switching the input signal for "black" and "white" .



【Note4】This shall be measured at center of the screen.

【Note5】Definition of white uniformity:

White uniformity is defined as the following with five measurements (A～E).



$$\delta_W = \frac{\text{Maximum Luminance of five points (brightness)}}{\text{Minimum Luminance of five points (brightness)}}$$

11. Display Quality

The display quality of the color TFT-LCD module shall be in compliance with the Incoming Inspection Standard.

12. Handling Precautions

a) Be sure to turn off the power supply when inserting or disconnecting the cable.

b) Be sure to design the cabinet so that the module can be installed without any extra stress such as warp or twist.

c) Since the front polarizer is easily damaged, pay attention not to scratch it.

d) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.

e) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.

f) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface. Handle with care.

g) Since CMOS LSI is used in this module, take care of static electricity and injure the human earth when handling.

h) Observe all other precautionary requirements in handling components.

i) This module has its circuitry PCBs on the rear side and should be handled carefully in order not to be stressed.

j) Laminated film is attached to the module surface to prevent it from being scratched . Peel the film off slowly just before the use with strict attention to electrostatic charges. Ionized air shall be blown over during the action. Blow off the 'dust' on the polarizer by using an ionized nitrogen gun, etc..

k) When handling LCD modules and assembling them into cabinets, please be noted that long-term storage in the environment of oxidization or deoxidization gas and the use of such materials as reagent, solvent, adhesive, resin, etc. which generate these gasses, may cause corrosion and discoloration of the LCD modules.

13. Packing form

a) Piling number of cartons: 5 cartons

b) Package quantity in one carton: 10 pcs

c) Carton size : 438(W)×355(D)×295(H)mm

d) Total mass of one carton filled with full modules: 7000g

14. Reliability test items

No.	Test item	Conditions
1	High temperature storage test	Ta = 60℃ 240h
2	Low temperature storage test	Ta = -25℃ 240h
3	High temperature & high humidity operation test	Ta = 40℃ ; 95 %RH 240h (No condensation)
4	High temperature operation test	Ta = 50℃ 240h (The panel temp. must be less than 60℃)
5	Low temperature operation test	Ta = 0℃ 240h
6	Vibration test (non- operating)	Frequency : 10～57Hz/Vibration width (one side):0.075mm : 58～500Hz/Gravity:9.8m/s^2 Sweep time : 11 minutes Test period : 3 hours (1 hour for each direction of X,Y,Z)
7	Shock test (non- operating)	Max. gravity : 490 m/s^2 Pulse width : 11 ms, sine wave Direction : ±X,±Y,±Z once for each direction.

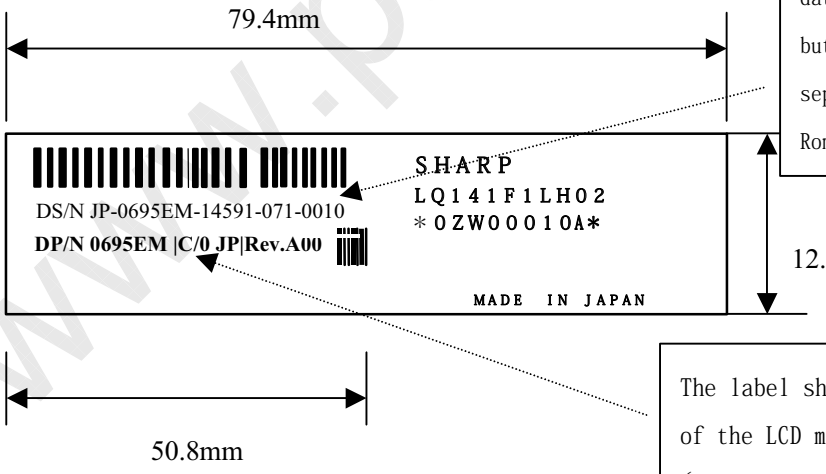
15. Bar code label

1) Printing Specification of module label (about the printing "DP/N 0695EM|C/O JP|Rev.A00")

Model ：LQ141F1LH02…DP/N695EM

Production Lot No.：(e.g.) Japan Product, 2000/6 Production Lot the 10th unit

Rev. ：A00



The barcode data and HRI of the barcode data should contain the same information, but HRI will contain a dash (-) to separate each field. (HRI = Times New Roman (Font) at a size of 7 points.)

The label should show the Country of Origin of the LCD module.
(Times New Roman (Font) at size of 8 points.)

The bar code size and information to be included:

- DS/N: 20-digit barcode(The longer and larger barcode on the upper side)：Code 128B
- DP/N: Rev(revision) barcode(The smaller barcode on the lower side)：Code 39
- Wide to narrow element ratio of 3 to 1
- The narrow element must be a minimum of 5 mils (0.127mm)

BAR CODE (UPPER SIDE)

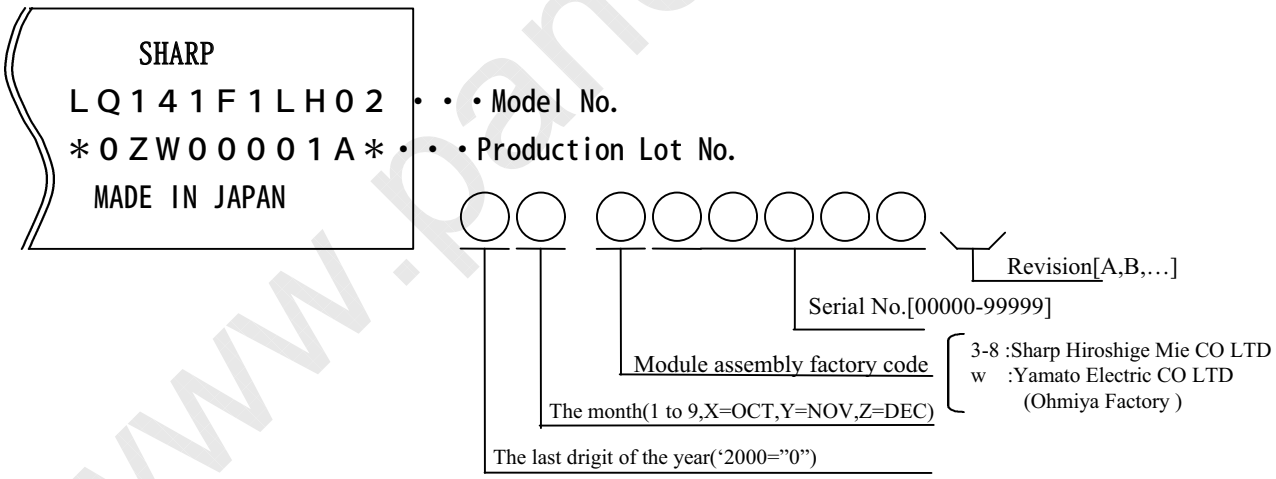
1st to 2th digit	(1)Country of Origin : "JP" for Japan made "TW" for SET(Taiwan) made
3st to 8th digit	(2) DELL Part Number: "(has been changed to 6-digit with only 1 leading "0")"
9th to 13th digit from the left	(3) Supplier ID: "14591"
14th digit	(4) the last digit of the year(with the dash"－" removed, this comes after the Supplier ID)
15th digit	(5) the month (1 to 9, A=OCT, B=NOV, C=DEC)
16th digit	(6) "1" (One) fixed
17th to 20nd digit	(7) 16 Repeated Counting Numbers (0000 to FFFF)

JP XXXXXX 14591 0 6 1 0010
(1) (2) (3) (4)(5)(6) (7)

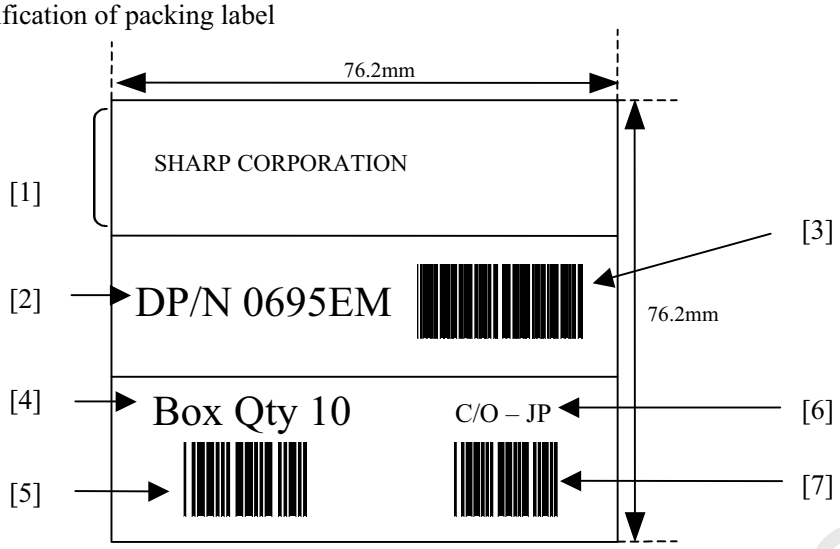
BAR CODE (LOWER SIDE)

Rev: Letter and Barcode = Fixed to "A00" for the moment

The right side of the bar code label shows Sharp's Specification:



2) Printing Specification of packing label



[1] Supplier Name [HRI]

[2] Dell Part Number[HRI]

[3] Dell Part Number[Barcode]:Code128B

- LQ141F1LH02 → 0695EM

[4] Box Quantity[HRI]

[5] Box Quantity[Barcode(Lower Left Side)]:Code 128B

- LQ141F1LH02 → 10

[6] Country of Origin[HRI]

[7] Country of Origin[Barcode(Lower right Side)]:Code 128B

- Japan → JP

16. Others

1) Adjusting volume have been set optimally before shipment, so do not change any adjusted value. If adjusted value is changed, the technical literature may not be satisfied.

2) Disassembling the module can cause permanent damage and should be strictly avoided.

3) Please be careful since image retention may occur when a fixed pattern is displayed for a long time.

4) If any problem occurs in relation to the description of this specification, it shall be resolved through discussion with spirit of cooperation.

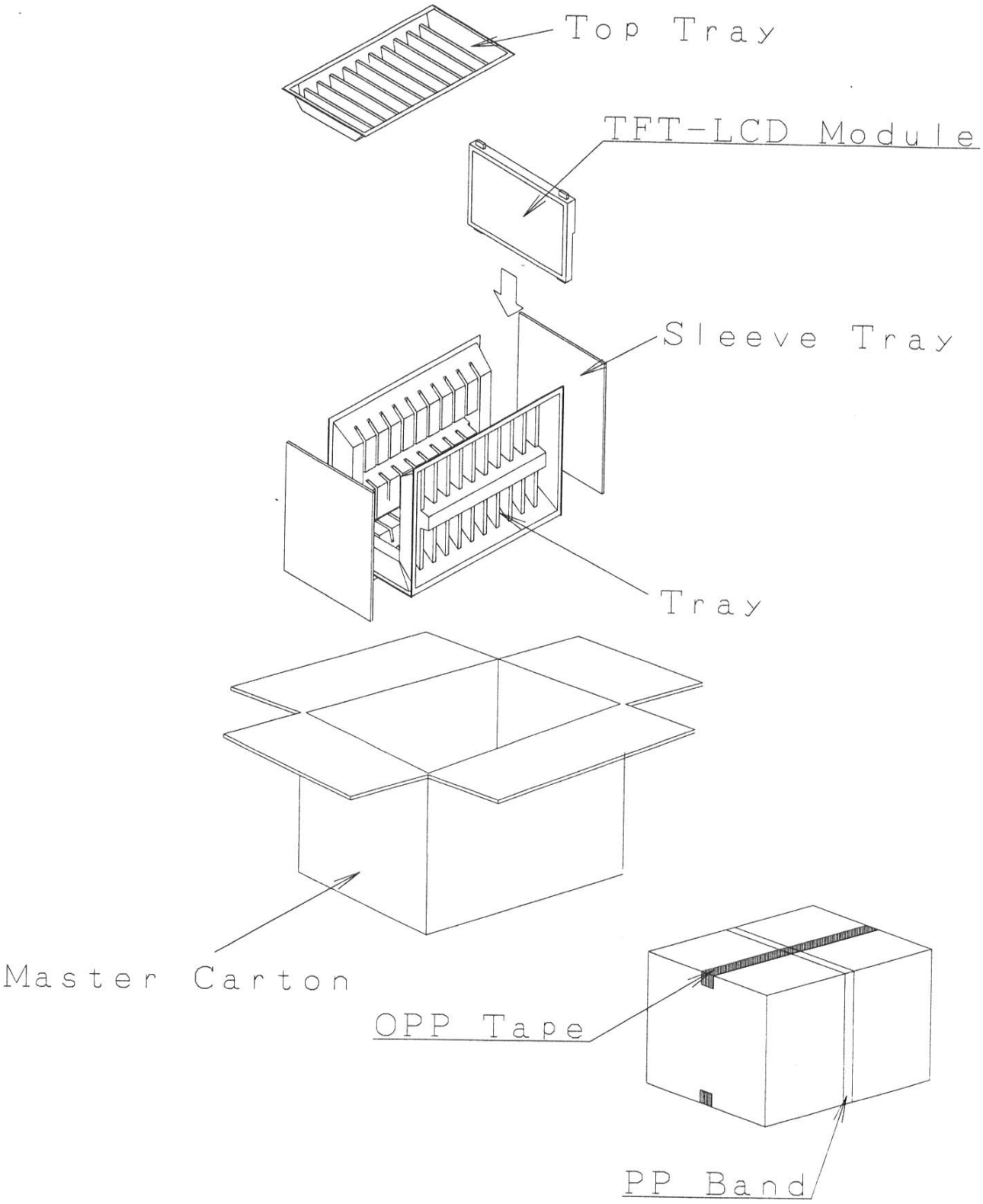


Fig3-1. Packing Form

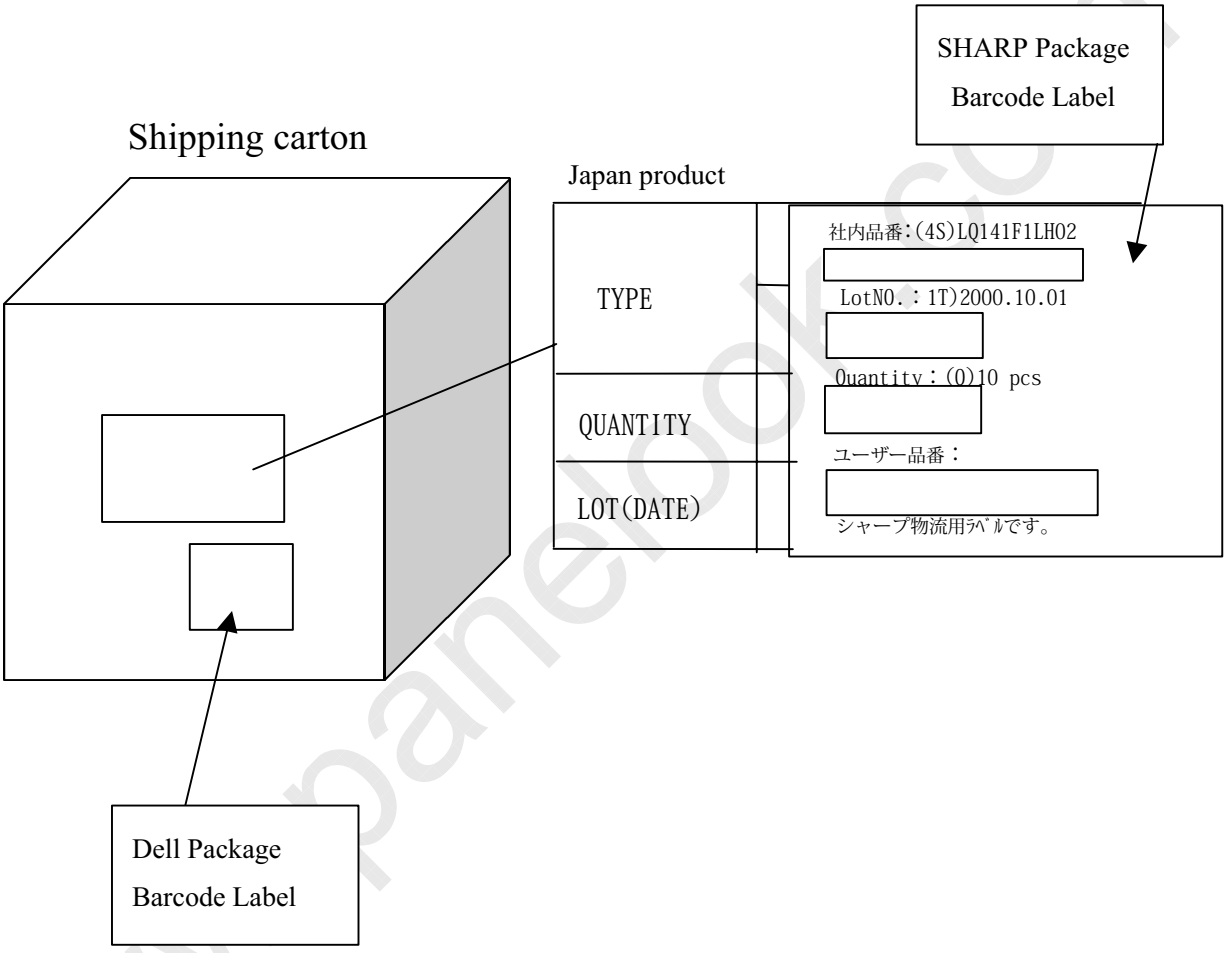
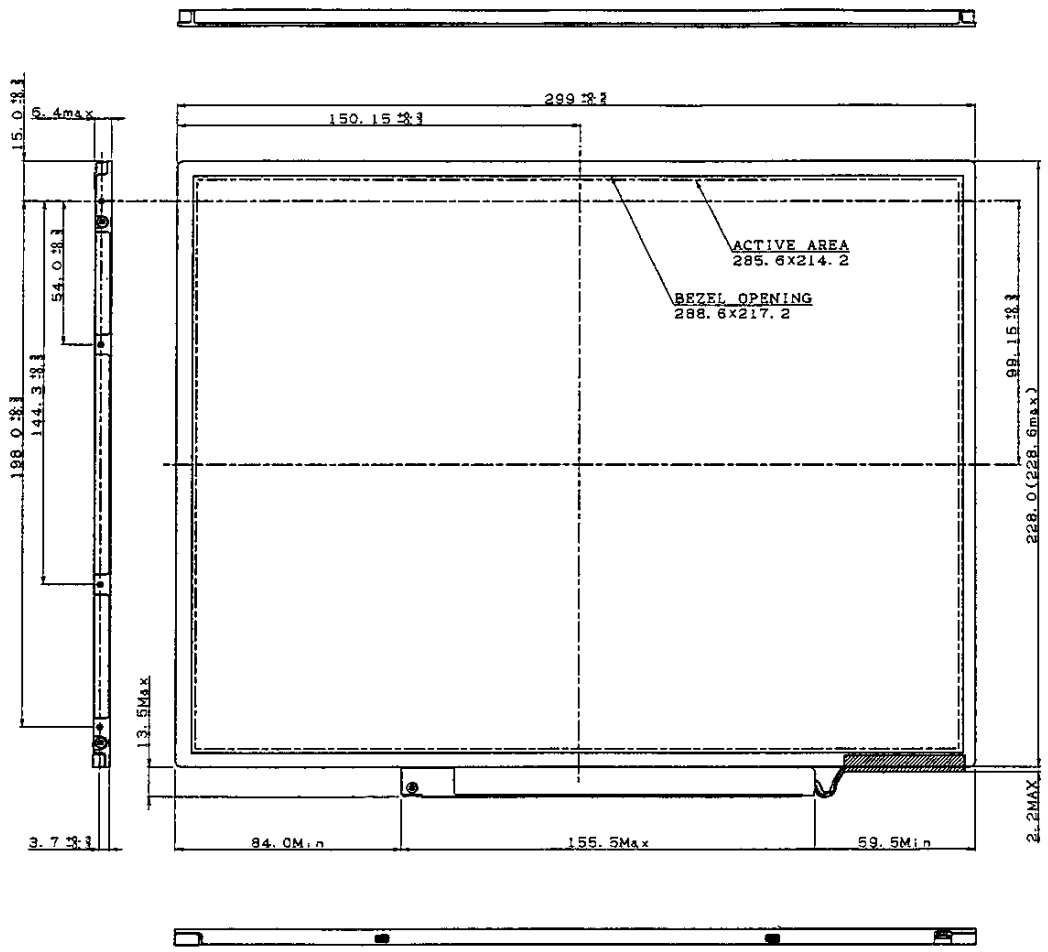
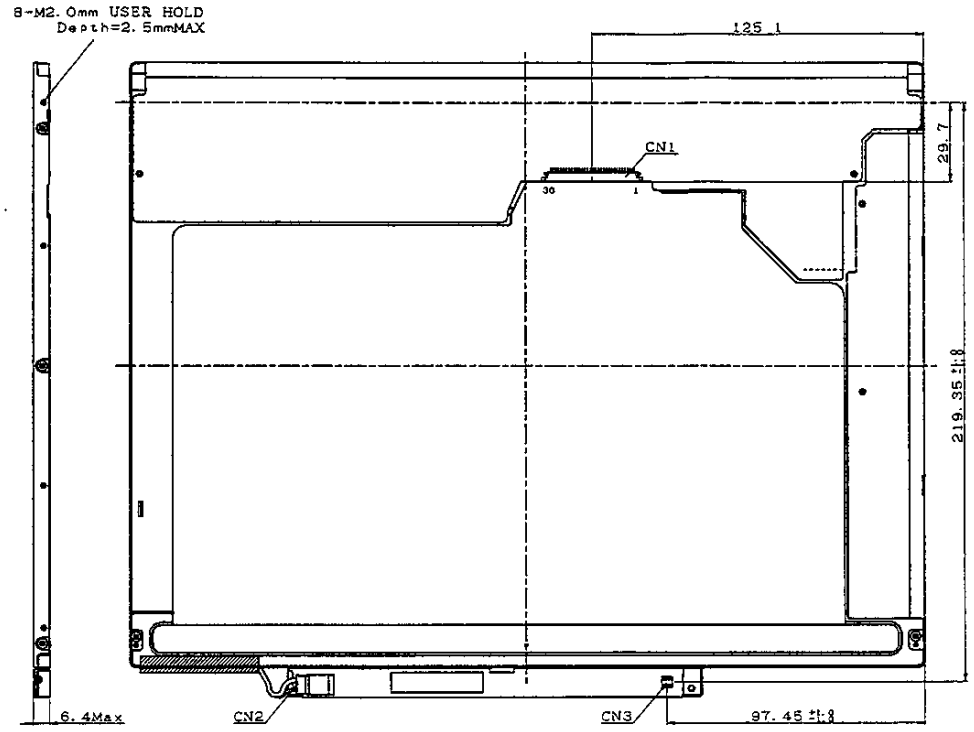


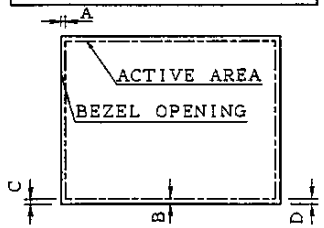
Fig3-2. Location of barcode label attachment





CN1 Pin Assign	
1	GND
2	VCC
3	VCC
4	Veded
5	NC
6	CLKedid
7	DATAedid
8	R1IN0-
9	R1IN0+
10	GND
11	R1IN1-
12	R1IN1+
13	GND
14	R1IN2-
15	R1IN2+
16	GND
17	CK1IN-
18	CK1IN+
19	GND
20	R2IN0-
21	R2IN0+
22	GND
23	R2IN1-
24	R2IN1+
25	GND
26	R2IN2-
27	R2IN2+
28	GND
29	CK2IN-
30	CK2IN+

BEZEL/DISPLAY POSITION



1)TOLERANCE X-DIRECTION A:1.5±0.5
2)TOLERANCE Y-DIRECTION B:1.5±0.5
3)OBLIQUITY OF DISPLAY AREA |C-D|<0.5

CN1:INTERFACE CONNECTOR
IF-XB30S-HF10(JAE)

CN2:CCFT CONNECTOR
BHSR-02VS-1(JST)

CN3:INVERTER CONNECTOR
WR-L16S-VF-1(JAE)

NOTES
1. UNSPECIFIED TOLERANCE TO BE ±0.5
2. WARP AND FLATING FOR
PCB AND CHASSIS ARE EXCLUDED FROM
THICKNESS AND DIMENSION OF THE UNIT.

LQ141F1LH02 OUTLINE DIMENSIONS

2D-007-744-02